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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,922	01/15/2004	Chris J. Newburn	42P17410	1517

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EXAMINER	
IWASHKO, LEV	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,922	NEWBURN ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because drawings 1-20 have hand-written items and references, making them informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-2 are rejected under U.S.C. 102(b) as being anticipated by Dye et al. (US Patent 6,145,069).

Claim 1. A processor *(Column 11, lines 15-19 – Declare a processor coupled to the cache memory)*

- comprising cache coherency rule logic circuitry, said cache coherency rule logic circuitry to label a cache line's worth of information in accordance with at least one cache coherency rule selected from the group consisting of: *(Column 13, lines 13-20 – State the following: "The Cache and Coherency Controller 370 couples to the compression/decompression Control logic 340, the compression overflow unit 310, and the Compression Cache Memory 160 for generation and notification for Compression Cache control. This unit 370 may contain tag address tables for cache hit/miss information and may also contain other logic necessary to control the system coherency")*

a) where said cache line's worth of information is a compressed cache line's worth of information that was written to with new information that allowed said compressed cache line's worth of information to remain compressed, keeping said compressed cache line's worth of information in the same state that it was in just prior to being written to; *(Column 5, lines 26-36 – Declare that compressed information is written and remains compressed)*

b) where said cache line's worth of information is an uncompressed cache line's worth of information that was spawned from a compressed cache line's worth of information that could not remain compressed after being written to with new information, *(Column 15, lines 38-52 – State that the compressed data de-compresses during the writing process)*

- labeling said uncompressed cache line's worth of information as being in a Modified state; and, *(Column 14, line 51 – States that the LRU/LMU state is updated)*

c) where said cache line's worth of information is a compressed cache line's worth of information created by compressing an uncompressed cache line's worth of information and a companion of said uncompressed cache line's worth of information, *(Column 16, lines 5-9 – State that decompressed data merges with the write data and becomes re-compressed)*

- labeling said compressed cache line's worth of information as being in a Modified state. *(Column 16, line 9 – States that the data is written back to memory upon modification)*

Claim 2. A processor comprising a hub to support said processor's participation in a multi-processor computing system that uses compressed cache lines' worth of information, said hub comprising: *(Figure 3 – Shows a hub)*

a) a first bus or link interface to couple to a component of said system that can not send and receive a compressed cache line's worth of information; *(Figure 3, Diagram 280 – Shows the Decompression engine that cannot receive a compressed cache line's worth of information)*

b) a second bus or link interface to couple to a component of said system that can send and receive a compressed cache line's worth of information; *(Figure 3, Diagram 260 – Shows the Compression Engine and how it can send a receive a compressed cache line's worth of information)*

c) a first data path from b) to a) comprising decompression logic circuitry; *(Figure 3, Diagrams 220, 280, and 160 – Demonstrate a path from the ECC/EDC logic to the Decompression Engine to the SRAM cache)*

d) a second data path from b) to a) that bypasses said decompression logic circuitry; *(Figure 3, Diagrams 220, 240, and 160 – Demonstrate a path from the ECC/EDC logic to the Bypass to the SRAM Cache)*

e) a first data path from a) to b) comprising a buffer and *(Figure 5, Diagram 160 – Shows a data buffer)*

- compression logic circuitry; and, (Figure 4, Diagram 260 – Shows the Compression Engine)

f) a second data path from a) to b) that comprises said buffer and that bypasses said compression logic circuitry. *(Figure 5, Diagrams 160 and 240 – Demonstrate a path from the data buffer to the bypass and so on...)*

4. Claim 3 is rejected under U.S.C. 102(e) as being anticipated by Naffziger et al. (US PGPub 2003/0135694).

Claim 3. A method, comprising:

- within a multi-processor computing system: *(Section 0016, lines 1-3 – State that many systems embody multiple-processors)*
- compressing a first cache line's worth of information and a second cache line's worth of information into a compressed cache line's worth of information, *(Sections 0032-0033 – State the following: "The compression engine periodically reads the cache line group, rewrites it in compressed form if data in the cache line group is compressible, and updates the compressed flags and way indicators of each associated tag line to indicate where in the cache line group each line of data is stored. In this embodiment, if some or all lines of the cache line group are stored in compressed form, the remaining space in the line group is usable by cache data associated with the excess address tags")*
- said first cache line's worth of information and said second cache line's worth of information being companions of one another. *(Section 0032, line 2 – Denotes a cache line group)*

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER